UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,050	12/29/2000	Pablo M. Rodriguez	42390P8929	8976

7590 12/12/2003

Jeffrey S. Draeger
Blakely, Sokoloff, Taylor & Zafman
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
LE, DIEU MINH T	
ART UNIT	**PAPER NUMBER**
2184	2

DATE MAILED: 12/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PPG

Office Action Summary	Application No.	Applicant(s)	
	09/751,050	RODRIGUEZ, PABLO M.	
	Examiner	Art Unit	
	Dieu-Minh Le	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,12,18-22 and 28-30* is/are rejected.

7)☒ Claim(s) *9,10 and 13-17* is/are objected to.

8)☒ Claim(s) *23-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/29/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Specification

1. Claims 1-30 are presented for examination.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-22, 28-30, drawn to apparatus and method for detecting and recovering from errors in a source synchronous bus, classified in class 714, subclass 56.

II. Claims 23-27, drawn to method for analyzing an internal clock signals, classified in class 713, subclass 500.

The inventions are distinct, each from the other because of the following reasons:

1. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention of Group I has separate utility such as bus agent capable of detecting a glitch on strobe signals and retrying the

transaction to retrieve data; this is a patentably distinct feature not found in invention II. See MPEP § 806.05(d).

2. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Mr. Jeffrey S. Draeger, Reg. No. 41,000 on November 26, 2003, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-22, 28-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23-27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 11-12, 18-22, and 28-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable Ilkbahar (US Patent 6,433,600) in view of Kurd et al. (US Patent 6,505,262 hereafter referred to as Kurd).

As per claim 1:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- an apparatus

comprising:

- a plurality of strobe inputs to receive a plurality of strobe signal [col. 1, lines 59-60];
- a plurality of data inputs to receive a plurality of data signals transmitted in a transaction in conjunction with plurality of strobe signals in a source synchronous manner [col. 4, lines 67 through col. 5, lines 12];
- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].

Ilkbahar does not explicitly teach:
- bus control logic to produce an external visible indication of errors occurred.

However, Ilkbahar does disclose capability of:
- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent [col. 2, lines 42-51];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7]; comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch [col. 7, lines 59-67].

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent as well as externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner** as being the bus control logic to produce an external visible indication of errors occurred as claimed by Applicant. This is because the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling. It is further obvious because the Ilkbahar illustrated and demonstrated the control logic communication to and from processing bus and other communication devices such as delay circuitry, glitch circuitry, etc.. in supporting the computer operation system; second, one would modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the capability of capturing data from a communication bus having**

plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) as well as detecting strobe glitches used in responding to error signal identifying a strobe glitch as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the data transmission system with plurality of communication devices and peripheral and more specifically to the source synchronous bus devices with a mechanism to enhance data or power transmission performance/monitoring, data availability/reliability, and data configuring/exchanging operation via ECC means for data recovery process. It is further obvious because by utilizing this approach, the source synchronous bus devices with a processor-based computer can be realized in high performance throughput with a high reliability and flexibility power transmission environment. That will correctly provide optimum wireless data availability and transmission throughput among end users real-time communication and execution.

As per claims 2-4:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- an apparatus

comprising:

- a plurality of strobe inputs to receive a plurality of strobe signal [col. 1, lines 59-60];
- data signals latched with glitch [col. 1, lines 65-67];
- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].

Ilkbahar does not explicitly teach:

- bus control logic to produce an external visible indication of errors occurred by retry the transaction.

However, Ilkbahar does disclose capability of:

- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent [col. 2, lines 42-51];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

- first and second latch circuits used to determining transition logic state ins responding to circuit detection [col. 8, lines 26-43].

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7]; comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)* [col. 7, lines 59-67].

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent as well as first and second latch circuits used to determining transition logic state in responding to circuit detection** as being bus control logic to produce an external visible indication of errors occurred by retry the transaction as claimed by Applicant. This is because the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling. It is further obvious because the Ilkbahar illustrated and demonstrated the re-trying transaction due by failure occurred within the control logic communication to and from processing bus and other communication devices via transition logic states

in supporting the computer operation system; second, one would modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the capability of capturing data from a communication bus having plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) as well as detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)*** as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the data transmission system with plurality of communication devices and peripheral and more specifically to the source synchronous bus devices with a mechanism to enhance data ECC means for data recovery process. It is further obvious because by utilizing this approach, the source synchronous bus devices with a processor-based computer can be realized in high performance throughput with a high reliability and flexibility environment.

As per claims 5-6:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- an apparatus

comprising:

- a plurality of strobe inputs to receive a plurality of strobe signal [col. 1, lines 59-60];
- data signals latched with glitch [col. 1, lines 65-67];
- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].
- to stop sending additional bus request, and to disregard data received in conjunction with transaction [col. 4, lines 26-39 and col. 4, lines 53-67]
- waiting until no further strobes are outstanding [col. 5, lines 46-63].

Ilkbahar does not explicitly teach:

- bus control logic to retry the transaction.

However, Ilkbahar does disclose capability of:

- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent [col. 2, lines 42-51];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

- first and second latch circuits used to determining transition logic state ins responding to circuit detection [col. 8, lines 26-43].

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7]; comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)* [col. 7, lines 59-67].

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent as well as first and second latch circuits used to determining transition logic state in responding to circuit detection** as being the bus control logic to retry the transaction as claimed by Applicant. This is because the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling. It is further obvious because the Ilkbahar illustrated and demonstrated the re-trying transaction due by failure occurred

within the control logic communication to and from processing bus and other communication devices via transition logic states in supporting the computer operation system; second, one would modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the capability of capturing data from a communication bus having plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) as well as detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)*** as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing for the same reasons set forth as described in claim 2, **supra.**

As per claim 7:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- a bus agent [col. 3, lines 39-44]

comprising:

- a plurality of strobe inputs to receive a plurality of strobe signal [col. 1, lines 59-60];

- a plurality of data inputs to receive a plurality of data signals [col. 4, lines 67 through col. 5, lines 12];

- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].

- a glitch protection circuit to monitor plurality of clock signals [col. 2, lines 42-51];

Ilkbahar does not explicitly teach:

- a state machine coupled to receive plurality of strobe signals and to generate a plurality of clock signal.

However, Ilkbahar does disclose capability of:

- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

- strobe signals logic state transitions between bus maters of source synchronous data transferring computer system [abstract, col. 2, lines 35-51]

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7]; comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch [col. 7, lines 59-67].

- generating of logical multiplication of the strobe signals [col. 2, lines 51-64];

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made

first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent as well as externally strobe signals logic state transitions between bus maters of source synchronous data transferring computer system** as being the state machine coupled to receive plurality of strobe signals and to generate a plurality of clock signal as claimed by Applicant. This is because the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling and its logic states ***(i.e., state machine).*** It is further obvious because the Ilkbahar illustrated and demonstrated the state machine by control logic communication to and from processing bus and other communication devices such as delay circuitry and glitch circuitry; second, one would modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the capability of capturing data from a communication bus having plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) as well as**

generating of logical multiplication of the strobe signals as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing communication networking environment.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the data transmission system with plurality of communication devices and peripheral and more specifically to the source synchronous bus devices with a mechanism to enhance data ECC means for data recovery process via the state logic or state machine capability or clock signaling.

As per claims 8, and 18:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- a bus agent [col. 3, lines 39-44]

comprising:

- a plurality of strobe inputs to receive a plurality of strobe signal [col. 1, lines 59-60];
- a plurality of data inputs to receive a plurality of data signals [col. 4, lines 67 through col. 5, lines 12];

- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].

- a glitch protection circuit to monitor plurality of clock signals [col. 2, lines 42-51];

Ilkbahar does not explicitly teach:

- a state machine to generate four non-overlapping clock signals.

However, Ilkbahar does disclose capability of:

- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

- strobe signals logic state transitions between bus maters of source synchronous data transferring computer system [abstract, col. 2, lines 35-51]

- different strobe clocking signals in supporting the source and non-source synchronous bus environment *(i.e., four non-overlapping clock signals)* [col. 5, lines 1-4].

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7]; comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch [col. 7, lines 59-67].

- generating of logical multiplication of the strobe signals [col. 2, lines 51-64];

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made

first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **different strobe clocking signals in supporting the source and non-source synchronous bus environment** ***(i.e., four non-overlapping clock signals)*** as being the state machine to generate four non-overlapping clock signals as claimed by Applicant. This is because the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling ***(i.e., non-overlapping clock signals).*** It is further obvious because the Ilkbahar illustrated and demonstrated the state machine by control logic communication to and from processing bus and other communication devices such as delay circuitry and glitch circuitry; second, one would modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the generating of logical multiplication of the strobe signals** as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing communication

networking environment for the same reasons set forth as described in claim 7, **supra.**

As per claims 11-12:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- a bus agent

comprising:

- a plurality of strobe inputs to receive a plurality of strobe signal [col. 1, lines 59-60];
- data signals latched with glitch [col. 1, lines 65-67];
- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].
- a delay circuit to receive first clock signal and to generate a delayed first clock signal [col. 6, lines 62 through col. 7, lines 5].

Ilkbahar does not explicitly teach:

- bus controller to retry a transaction.

However, Ilkbahar does disclose capability of:

- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent [col. 2, lines 42-51];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

- first and second latch circuits used to determining transition logic state ins responding to circuit detection [col. 8, lines 26-43].

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7];

comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)* [col. 7, lines 59-67].

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

- a delay circuit to receive first clock signal and to generate a delayed first clock signal [col. 2, lines 55-64].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent as well as first and second latch circuits used to determining transition logic state in responding to circuit detection** as being the bus controller to retry a transaction as claimed by Applicant. This is because

the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling. It is further obvious because the Ilkbahar illustrated and demonstrated the re-trying transaction due by failure occurred within the control logic communication to and from processing bus and other communication devices via transition logic states in supporting the computer operation system; second, one would modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the capability of capturing data from a communication bus having plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) as well as detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)*** as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing for the same reasons set forth as described in claim 2, **supra.**

As per claim 19:

Ilkbahar substantially teaches the invention. Ilkbahar teaches:

- a system

comprising:

- a first and second bus agent capable of generating data signal and strobe signals for source synchronous transaction [col. 1, lines 59-60 and col. 3, lines 39-57];
- data signals latched with glitch [col. 1, lines 65-67];
- error detection if a glitch on one or more plurality of strobe signals detected [abstract, col. 2, lines 49-51].

Ilkbahar does not explicitly teach:

- bus agent to retry a transaction.

However, Ilkbahar does disclose capability of:

- a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus [abstract, col.1, lines 10-12]

comprising:

- a data network transmission connectivity among plurality of CPU, processor, processor bus, control device, chip set, etc... [fig. 1a-1b and 2, col. 2, lines 52 through col. 3, lines 67];

- a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent [col. 2, lines 42-51];

- externally connectivity to and from bus agent in supporting the computer system with higher performance bus architecture in synchronous manner [col. 3, lines 28-43].

- first and second latch circuits used to determining transition logic state ins responding to circuit detection [col. 8, lines 26-43].

In addition, Kurd explicitly teaches:

- a processing system having a glitch protection and detection for strobed data [abstract, col. 1, lines 5-7]; comprising:

- a method of capturing data from a communication bus [col. 7, line 35] having

- plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) [col. 7, lines 45-50].

- detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)* [col. 7, lines 59-67].

- a connectivity among inverting delay circuit, glitch protector circuit, counter, transition detector [col. 2, lines 51 through col. 3, line 63].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment including processor bus comprising **a glitch protection circuit and a detection circuits used to protect and detect signals corresponding to bus agent as well as first and second latch circuits used to determining transition logic state in responding to circuit detection** as being the bus agent to retry a transaction as claimed by Applicant. This is because the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment clearly perform the error detection and correction within the source synchronous bus area via plurality of strobes signaling. It is further obvious because the Ilkbahar illustrated and demonstrated the re-trying transaction due by failure occurred within the control logic communication to and from processing bus and other communication devices via transition logic states in supporting the computer operation system; second, one would

modify the Ilkbahar's a method and apparatus for glitch protection for input buffers in a source-synchronous environment to explicitly including **the capability of capturing data from a communication bus having plurality of strobe signaling and its transition occurring due to disabling (i.e., error occurrences) as well as detecting strobe glitches used in responding to error signal identifying a strobe glitch *(i.e., retry transaction)*** as taught by Kurd's processing system having a glitch protection and detection for strobed data in supporting the error detection and correction via a strobes signaling processing .

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the data transmission system with plurality of communication devices and peripheral and more specifically to the source synchronous bus devices with a mechanism to enhance data ECC means for data recovery process. It is further obvious because by utilizing this approach, the source synchronous bus devices with a processor-based computer can be realized in high performance throughput with a high reliability and flexibility environment.

As per claims 20-22:

Due to the similarity of claims 20-22 to claims 5-6; therefore, these claims are also rejected under the same rationale applied against claims 5-6. **In addition, all of the limitations have been noted in the rejection as per claims 5-6.**

As per claims 28-30:

Due to the similarity of claims 28-30 to claims 1-6 except for a method comprising steps of requesting data, receiving data, detecting a glitch, retrying a transaction, etc… instead of an apparatus comprising capabilities of receiving data, detecting a glitch, retrying a transaction, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-6. **In addition, all of the limitations have been noted in the rejection as per claims 1-6.**

Allowable Subject Matter

5. Claims 9-10, 13-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703) 305-9408. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel, can be reached on (703)305-9713. The fax phone number for this Group is (703)746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, n2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2184

DML
12/9/03